1.1. SHIELDING

Enclosed structure (equipment box or chassis in outside RF environment) should provide at least 100 dB of RF shielding at 1 MHz, 40 dB at 1 GHz.

Any opening in the surface of a shielded enclosure will allow electromagnetic energy to propagate into the enclosure, thus significantly reducing its shield integrity.

Use twisted shielded wire pairs, wherever possible to reduce coupling onto harnesses.

Make sure both ends of the cable are grounded in a 360 degree bond around the connector backshell. Do not open one end.

High shielding effectiveness may be obtained by using Class 3 chromate conversion finishes at joint seams of equipment boxes.

Make sure bolt attachment methods that do not penetrate the structure. Use dead-ended holes at module splices. Access doors should be held in place by a series of flush screws spaced as close together as possible. The proper torque should be applied to the bolt to avoid “oil canning”

Remember a paint can lid is the best form of sealing a joint against RF. If possible, use a dovetail type of joint to increase shielding effectiveness. RF does not like right angles. The more right angles the RF has to pass through to get to the electronics the more it will be attenuated.

All apertures should be made as small as possible.

Any windows should be designed to provide adequate shielding. Several special coatings are available for this application.

All desiccant openings should be as small as possible. Shielding control can be maintained by configuring the aperture as a waveguide-beyond-cutoff by properly selecting the dimensions of the aperture.

Any conductive gasket or sealant compounds (including their interfacing conductive surfaces at the metal-to-metal interfaces) that are exposed to moisture must be protected to avoid corrosion, particularly in a salt fog environment.

Pigtails on the shields should be avoided.

1.2. GROUNDING
A hybrid single-point grounding system should be used, which provides a short multipoint ground reference for all equipments within a system. The exception to this is transmitters can be grounded to its case. The corresponding antennas must be connected to ground unless designed otherwise.

There are several types of grounds; chassis, signal and power. Chassis ground is directly bolted to the frame of the box. Signal and power grounds are routed through the harness back to the single point ground.

1.3. PCB TRACE/COMPONENT LAYOUT

The motherboard should be a multilayer design such that the digital layers are separated by full power and ground planes. This separation shall be achieved by implementing both power and ground planes, consisting of one ounce copper (typical) but no less than 0.5 ounce copper, between digital layers such that the stack up consists of (Pad/Ground, Signal, Power, Signal, Signal, Ground, Signal, Pad/Ground). When two signal layers are back to back the traces shall run perpendicular to each other.

Any analog sections should be physically separated from digital sections of PCB’s within their own respective zones. This ‘Zoning’ should prevent the ‘mirror image’ current of digital traces from flowing in the analog zone of any analog to digital (A/D) circuits.

The physical layout for all traces should be designed such that they are routed over a continuous ground or power plane along their full length.

Any PCB ground planes that are cut, or somehow separated into digital and analog ground planes, should have a short bond between the analog and digital sections at the A/D converters. This short bond path should be wide enough to ensure that all digital and analog traces are routed adjacent to a continuous ground plane along the full length of their route.

All power and ground planes should extend continuously throughout all connector pin-out regions of each PCB, including the motherboard, and should not be interrupted in the connector region. In the connector region all ground and power planes should be interweaved throughout the connector region to ensure that the traces routed between connector pins have a continuous ground or power plane.

Circuit loop area should be minimized by employing full ground planes for both analog and digital circuits.

All components/connectors should be mounted such that ground planes remain around the entire perimeter of each pad and via. This is especially important for components whose pad spacing and via center to center spacing is 0.050 inches or less.

The PCB ground planes should extend within the connector region utilizing an ‘interweaving’ technique, whereby the signal/ground plane traces ‘weave’ through the connector region.
Where high speed devices (< 2 ns risetime and >10 MHz) are located close (within ~1 inch) to PCB connector pins, provisions for adding a ‘fence’ should be implemented to prevent device to pin coupling. The fence shall be composed of a vertical metallic barrier, connected to the PCB ground plane, and ‘covering’ the exposed connector pins. The fence should have ground pins (and associated vias) spaced one inch or less.

SMT devices, including connectors that use pad spacing of less than 0.1 inches, should stagger the pads to ensure that both the power and ground planes are continuous (not interrupted) around all pads and their associated vias.

All PCB signal traces should be approximately 0.0005 inch from the edge of the ground plane and/or power plane of the PCB.

All clock traces should be ‘sandwiched’ between two power/ground planes (stripline preferred) or adjacent to a power/ground plane (microstrip).

Short SMT clock traces shall run directly on the top side (‘microstrip’ i.e., without going through vias) from the microprocessor oscillator to the microprocessor chip. “short” is defined as less than one fortieth of a wavelength of the clock bandwidth (e.g., for risetime tr=1.5 ns the bandwidth is $1/\pi tr \approx 200$ MHz therefore $\lambda/40$ of 200 MHz $\approx 3.8$ cm or 1.5 inches) Clock traces longer than the $\lambda/40$ criteria should run as stripline, sandwiched between two planes.

Clock fan out shall be either ‘daisy chained’ or ‘parallel’, without using ‘stub type’ traces.

If daisy chaining of the clock signal is used then it is best to avoid a long straight line run; for this case it is best to ‘cluster’ together the devices receiving the clock signal (to minimize the linear length of any given clock trace in any given direction)

For short trace lengths, unterminated lines are acceptable when the two way propagation delay time is less than the signal-clock risetime (note: the velocity of propagation in air is the speed of light or $\approx 12$ inches/ns but in G10 PCB’s the velocity is $\approx 1/2$ the speed of light or 6 inches/ns).

Clock runs shall be terminated, where the two way propagation delay exceeds the clock risetime. Resistive, R-C, or diode terminations are acceptable. Termination resistance up to twice the trace characteristic impedance is acceptable.

Crosstalk control between digital traces is best achieved by physical spacing between traces. For clock traces the trace edge to edge separation distance, $S$, shall be a minimum of three times the trace height, $H$, hence $S/H>3$. For data traces, $S/H>1$. Guard traces are not recommended for digital crosstalk control.

All high speed devices shall be located a minimum of one inch from all connector, to reduce direct coupling between the device and the connector pins.
All high speed digital traces longer than 1.5 inches shall avoid trace crossovers, vias and trace width variations throughout their route, to reduce reflective noise due to impedance variations.

When making right angle trace bends choose: a) two 45 degree bends, b) miter the outside corner of the bend, or c) implement the bend using a smooth 90 degree arc.

1.4. PCB FILTERING REQUIREMENTS

The input power to each PCB shall be capacitively filtered (20 dB at 100 kHz) using a bulk storage electrolytic capacitor at the point of power entry. The capacitor value should all be $C=16/R \mu F$, where $R$ is the DC load resistance, or 10 $\mu F$, whichever is greater.

A 0.1 $\mu F$ low loss ceramic capacitor, preferably SMT, shall be implemented in parallel and immediately adjacent to the bulk storage electrolytic capacitor (noted above).

Localized component filtering shall also be provided by 0.001 $\mu F$ low loss ceramic capacitors, preferably SMT. Every three components shall have a minimum of one 0.001 $\mu F$ filter capacitor. The maximum separation distance between a Vcc/ground pins and the capacitor should not exceed 1.5 inches.

Note: the above filter is consistent with the minimum capacitor value separation needed to preclude self resonance thus each capacitor shall be different by at least two orders of magnitude.

1.5. CABLE DESIGN

Whenever possible, wiring should be categorized to isolate noisy (power) circuits from sensitive (signal) circuits. Place like wires together and isolate from others; (i.e., analog, digital, or power).

Pyrotechnic cabling is kept physically separated from other cabling.

Connector shells are considered to be a part of the cable shielding and shall be electrically conductive to the equipment case. All shields should be grounded at both ends at each bulkhead connector, and backshells with 360 degree shield terminations are used.

EED firing circuits employ twisted, shielded pairs & quads back to the control circuit. The shielding minimizes electric pickup, and the twisting reduces magnetic field pickup. This also reduces coupling into other nearby circuits.

1.6. CORROSION CONTROL

The equipment sections and access doors must be conductive at joints and other structural discontinuities. These requirements dictate careful corrosion protection procedures to
adequately protect the areas from corrosion. Avoid hard anodizing structure components separately then bolting together since anodizing does not provide for electrically conductive bonding at seams and joints.

Avoid the use of dissimilar metals.

1.7. TRANSIENT CONTROL

Suppress the transient at its source with voltage limiters. There are several types: silicon diodes, RC snubbers or Pi filters.

Slow down the response time of the digital devices until they cannot respond to typically fast transients.

Design a near zero impedance, equipotential Reference Ground Plane (RGP) directly accessible to all circuit elements without the use of round wires if possible.

Termination points that generally require protection are terminals on sensitive devices (integrated circuits, discrete components) or terminals on the interface of a shielded enclosure containing sensitive devices. In high peak voltage environments, such as switching transients, electrostatic discharge, lightning, and nuclear EMP, voltage limiters or termination protection devices (TPDs) are generally recommended and in many cases are mandatory to protect sensitive elements of a system from permanent damage.

Switch bounce, noisy power supplies and DC/DC converters produce unwanted noise.

1.8. ELECTROEXPLOSIVE DEVICE (EED)/ELECTRICALLY INIATIATED DEVICE (EID)

EED’s must be shielded with at least one enclosure.

Leads must be filtered at least at their entry points on the final shield enclosure.

Each line-pair leading to an EED must be dedicated to one EED and must be independent of other circuits, at least to the fire switch.

Note: E3 terms are defined in ANSI C63.14.